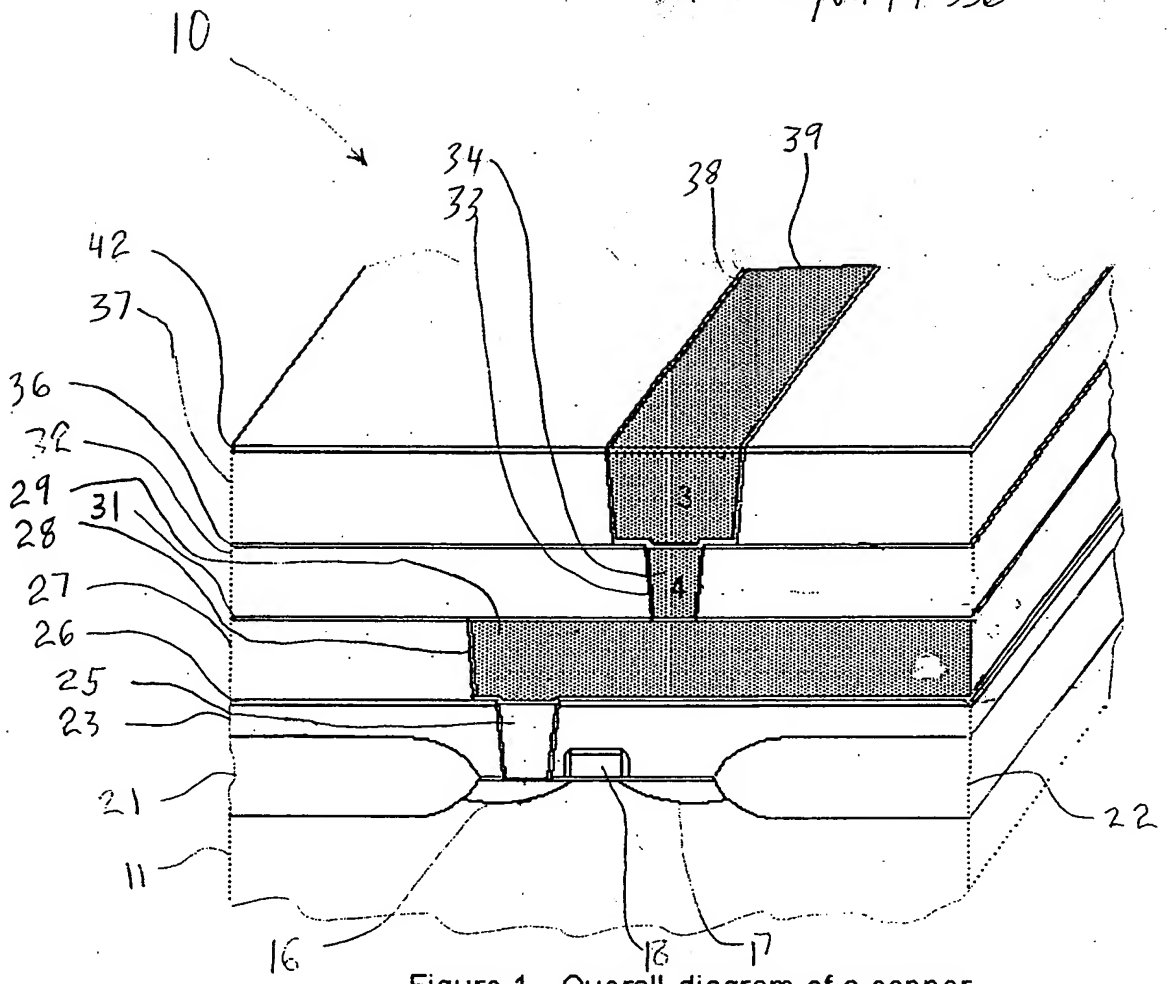
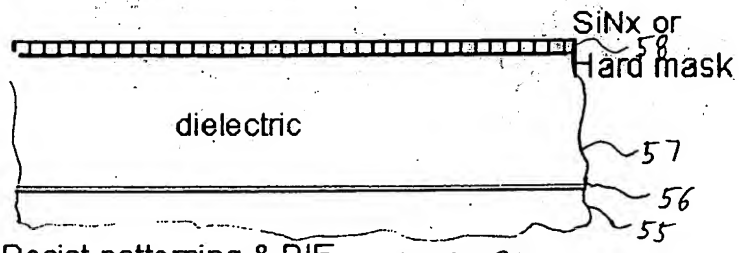


Figure 1 - Overall diagram of a copper interconnection structure

Process sequence 1: Single Damasceme

Deposited dielectric materials



Resist patterning & RIE

FIG 2A

etch via holes or lines

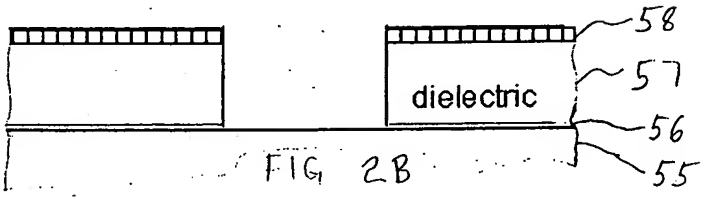


FIG 2B

Fill metals & CMP to remove excess metals

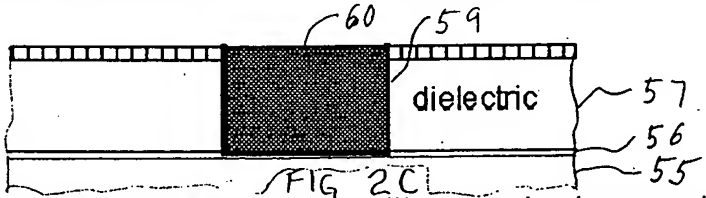


FIG 2C

Selective electroless deposition capping layer on top of Cu

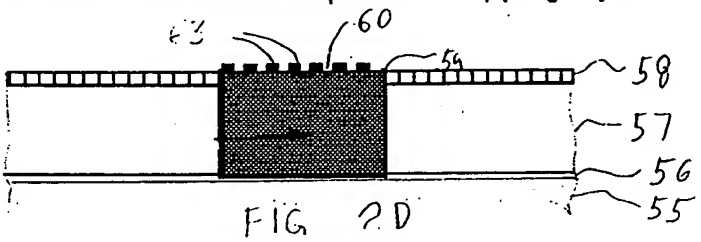


FIG 2D

SHEET 3 of 5
C.K. HU ET AL
RMT 10914-336

Process sequence 2: Dual Damascene

1. Deposit planar dielectric to a height of via + line

should be straight Horizontal lines

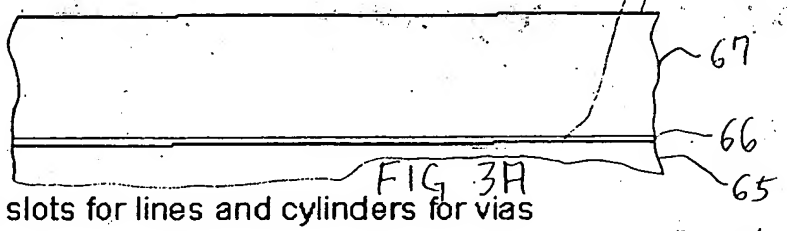
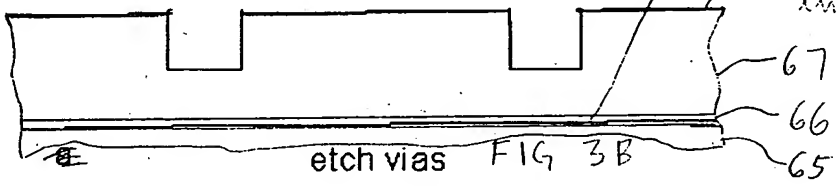


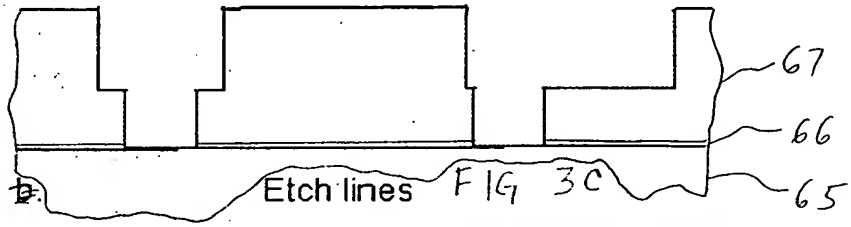
FIG 3A

2. Etch slots for lines and cylinders for vias

should be straight horizontal lines



etch vias FIG 3B



Etch lines FIG 3C

3. Fill etched pattern with metal, remove surplus from surface

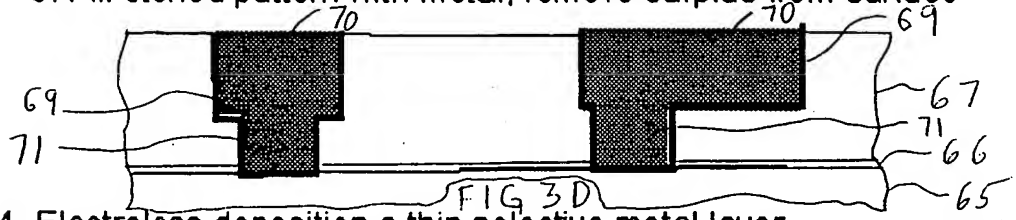


FIG 3D

4. Electroless deposition a thin selective metal layer

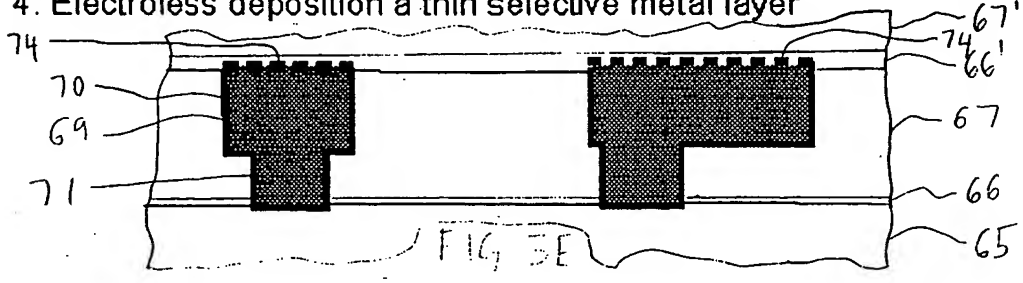


FIG 3E

SHEET 4 OF
C.K. HU ET AL
RMT Y0999-336

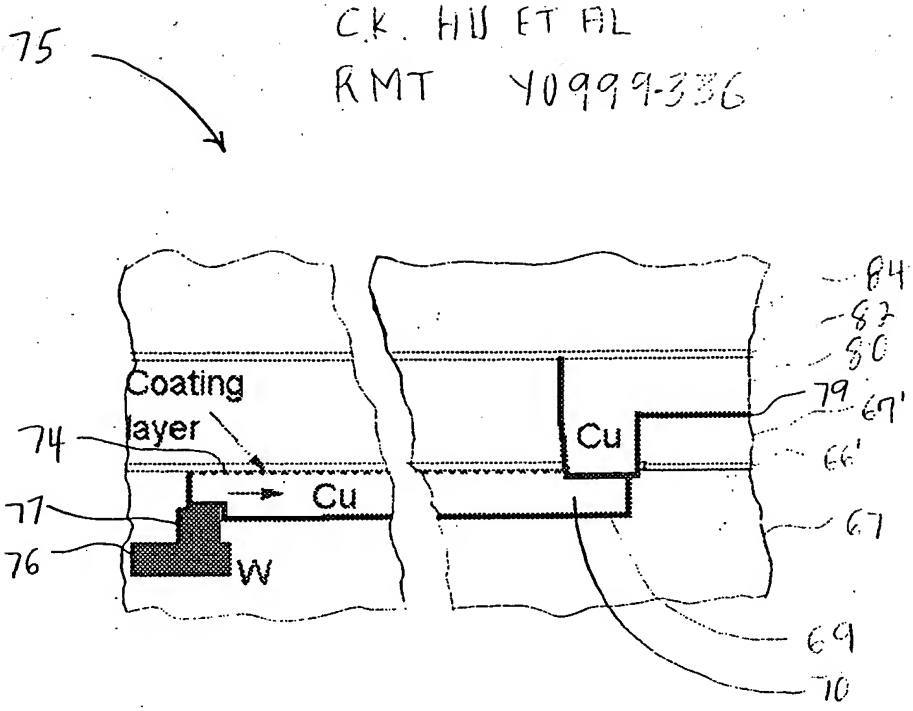


FIG 4

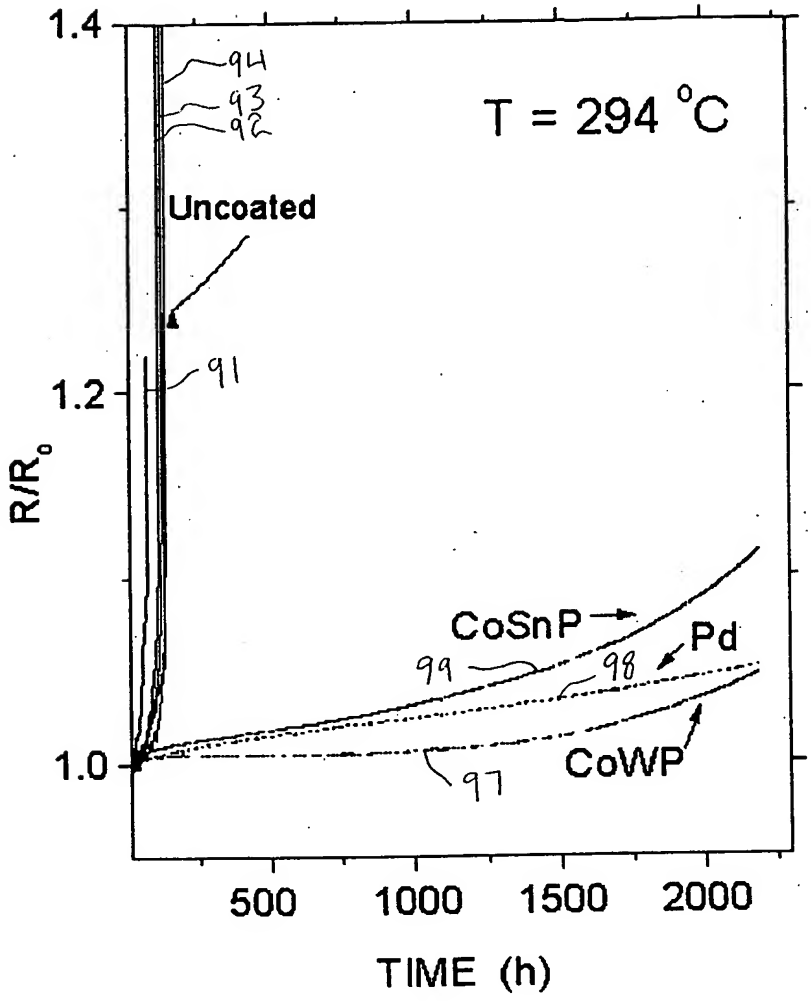

1.4
1.2
1.0
R/R$_o$
94
93
92
T = 294 °C
Uncoated
91
CoSnP
Pd
99
98
97
CoWP
500
1000
1500
2000
TIME (h)

FIG 5